Designing Sequential Circuits

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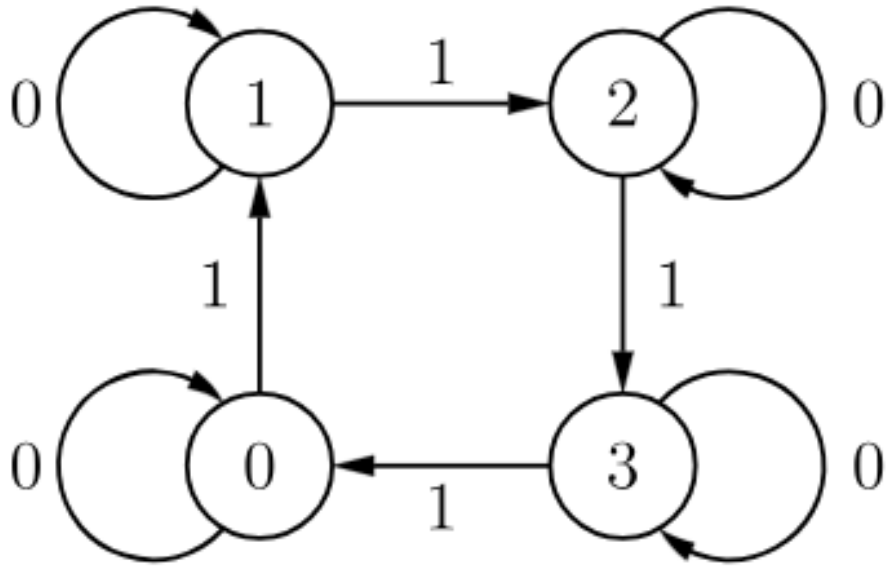
Steps in Designing Sequential Circuits

1. Create a state table and/or state diagram
2. Create binary-code for the state table and/or state diagram
3. Choose a type of flip-flop
4. Add columns to the state table that show the input required for each flip flop, to effect each required transition
5. Simplify each flip-flop input(s)
6. Draw the circuit

Example

Design a counter that has an *Enable* input When *Enable = 1* it increments through the sequence *0,1,2,3,0,1,...* with each clock tick. *Enable = 0* causes the counter to remain in its current state.

1. State Diagram



1. State Table

	$Enable = 0$	$Enable = 1$
Current	Next	Next
n	n	n
0	0	1
1	1	2
2	2	3
3	3	0

2. Binary Code for the State Table

N states required $log_2 N$ bits

E.g 4 states = 2 bits

Current		$Enable = 0$ Next		$Enable = 1$ Next	
n_1	n_0	n_1	n_0	n_1	n_0
0	0	0	0	0	1
0	1	0	1	1	0
1	0	1	0	1	1
1	1	1	1	0	0

3. Choose a Flip-flop

- Any flip-flop can be used
- If in doubt use J-K flip-flops for their general use cases
- I this example we will use the JK flip-flop

4. Add Columns for Flip-flop Inputs

- Consult the excitation tables for the chosen flip flop

Current		$Enable = 0$ Next						$Enable = 1$ Next					
n_1	n_0	n_1	n_0	J_1	K_1	J_0	K_0	n_1	n_0	J_1	K_1	J_0	K_0
0	0	0	0	0	X	0	X	0	1	0	X	1	X
0	1	0	1	0	X	X	0	1	0	1	X	X	1
1	0	1	0	X	0	0	X	1	1	X	0	1	X
1	1	1	1	X	0	X	0	0	0	X	1	X	1

Q n	Q n+1	J	K
0	0	0	X
1	0	X	1
0	1	1	X
1	1	X	0

5. Simplify the Flip-Flop Input(s)

- We can use Karnaugh maps

$J_0(E, n_1, n_0)$

E \ n_1n_0	00	01	11	10
0		X	X	
1	1	X	X	1

$K_0(E, n_1, n_0)$

E \ n_1n_0	00	01	11	10
0	X			X
1	X	1	1	X

$J_1(E, n_1, n_0)$

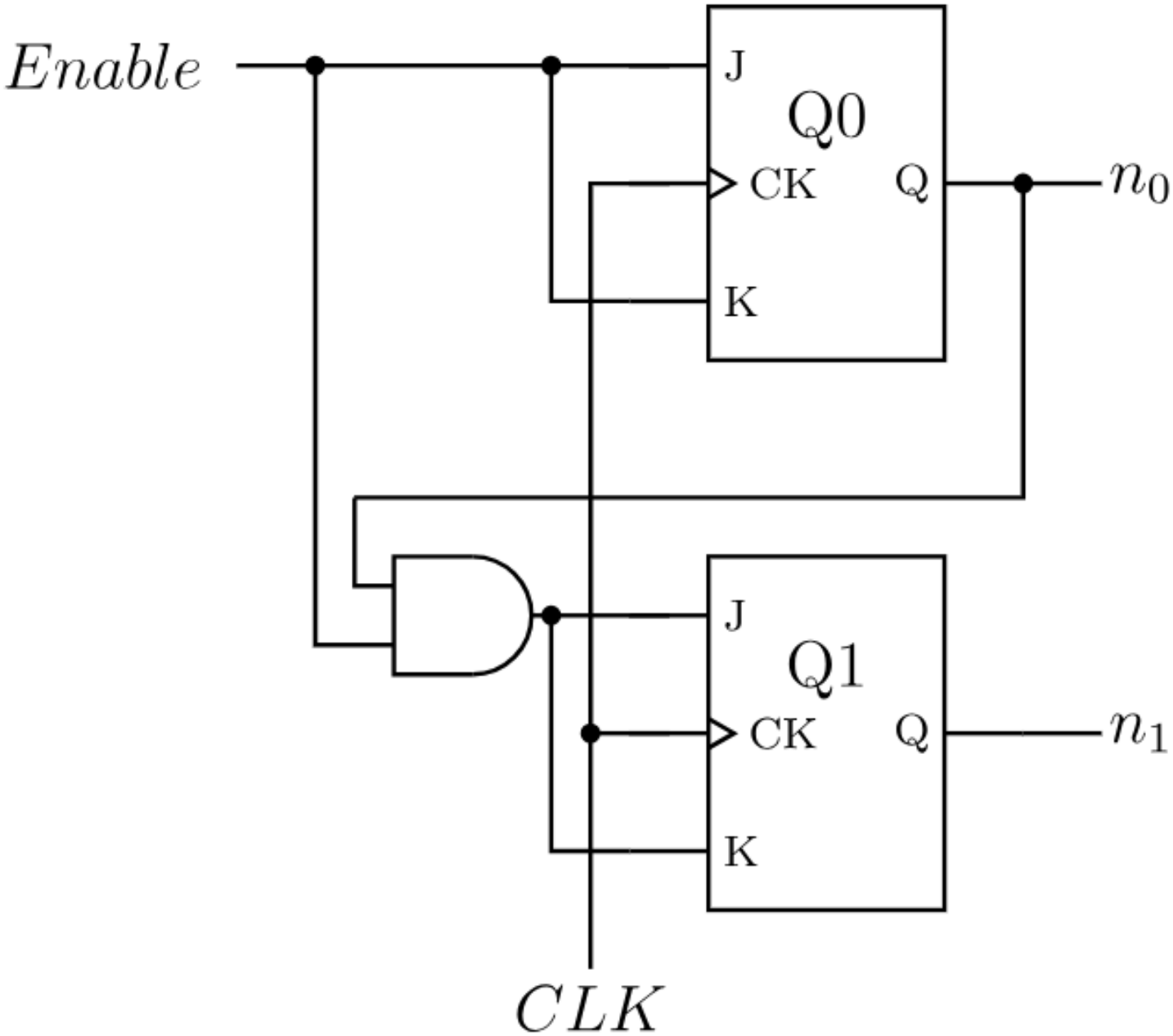
E \ n_1n_0	00	01	11	10
0			X	X
1		1	X	X

$K_1(E, n_1, n_0)$

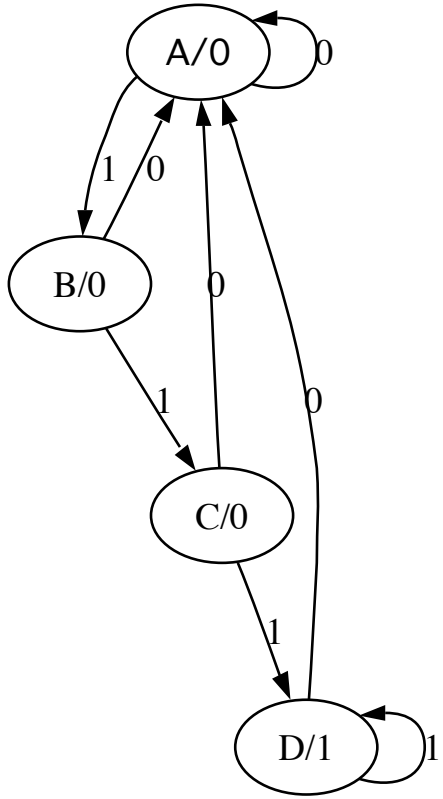
E \ n_1n_0	00	01	11	10
0	X	X		
1	X	X	1	

$$J_0(E, n_1, n_0) = E$$
$$K_0(E, n_1, n_0) = E$$
$$J_1(E, n_1, n_0) = E \cdot n_0$$
$$K_1(E, n_1, n_0) = E \cdot n_0$$

6. Draw the Circuit



Example



- explain the state diagram
- what is the output given the input sequence: 0011011111001011111?
- assume it starts in sate ”A”

Next State Table

q	$x = 0$	$x = 1$	z
A	A	B	0
B	A	C	0
C	A	D	0
D	A	D	1

- the information on the next state table is the same as in the FSM diagram
- Next step: state assignment
- how many bits do we need to keep track of the states?

State Assignment

A possible state assignment

q	q_1	q_2
A	0	0
B	0	1
C	1	0
D	1	1

- how many state assignments are possible?
- are some better than others?

Design Truth Table

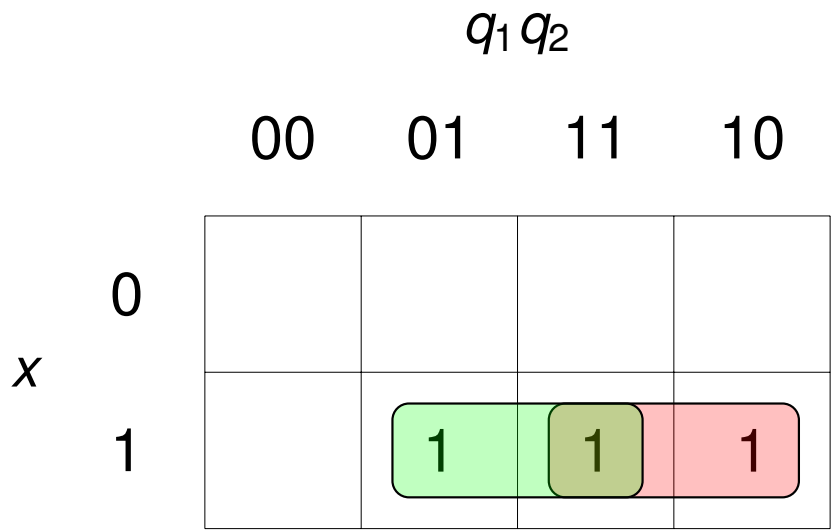
q	x	q_1	q_2	q_1^*	q_2^*
A	0	0	0	0	0
B	0	0	1	0	0
C	0	1	0	0	0
D	0	1	1	0	0
A	1	0	0	0	1
B	1	0	1	1	0
C	1	1	0	1	1
D	1	1	1	1	1

Design the circuit

- implement the FSM using D-FF
- Draw a Karnaugh map for q_1^* and q_2^*
- Draw a Karnaugh map for the output
- find the equations
- draw the circuit
- this is known as a Moore Machine (the output depends on the current state only)

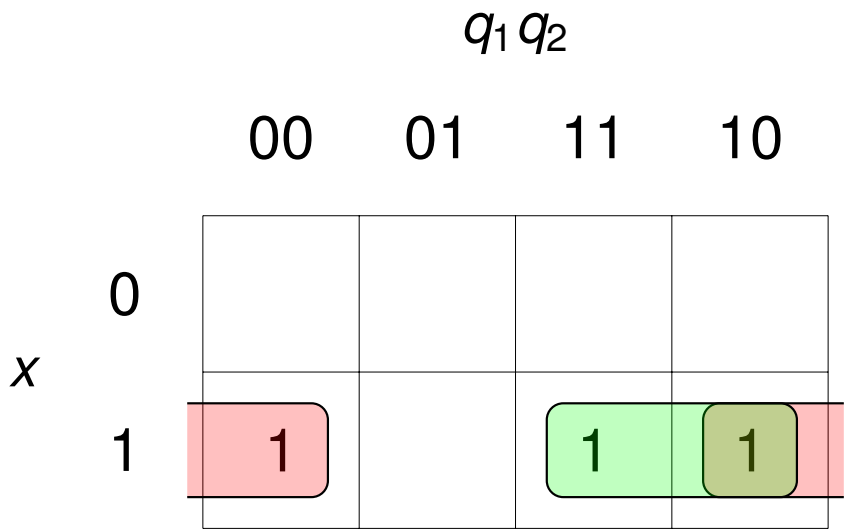
D-FF equations

From the truth table (see 2 slides back) write the Karnaugh maps.



$$q_1^* = xq_1 + xq_2$$

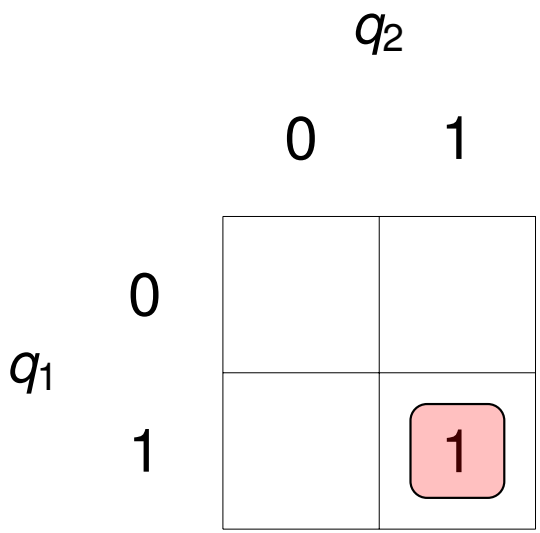
D-FF equations



$$q_2^* = xq_1 + x\overline{q_2}$$

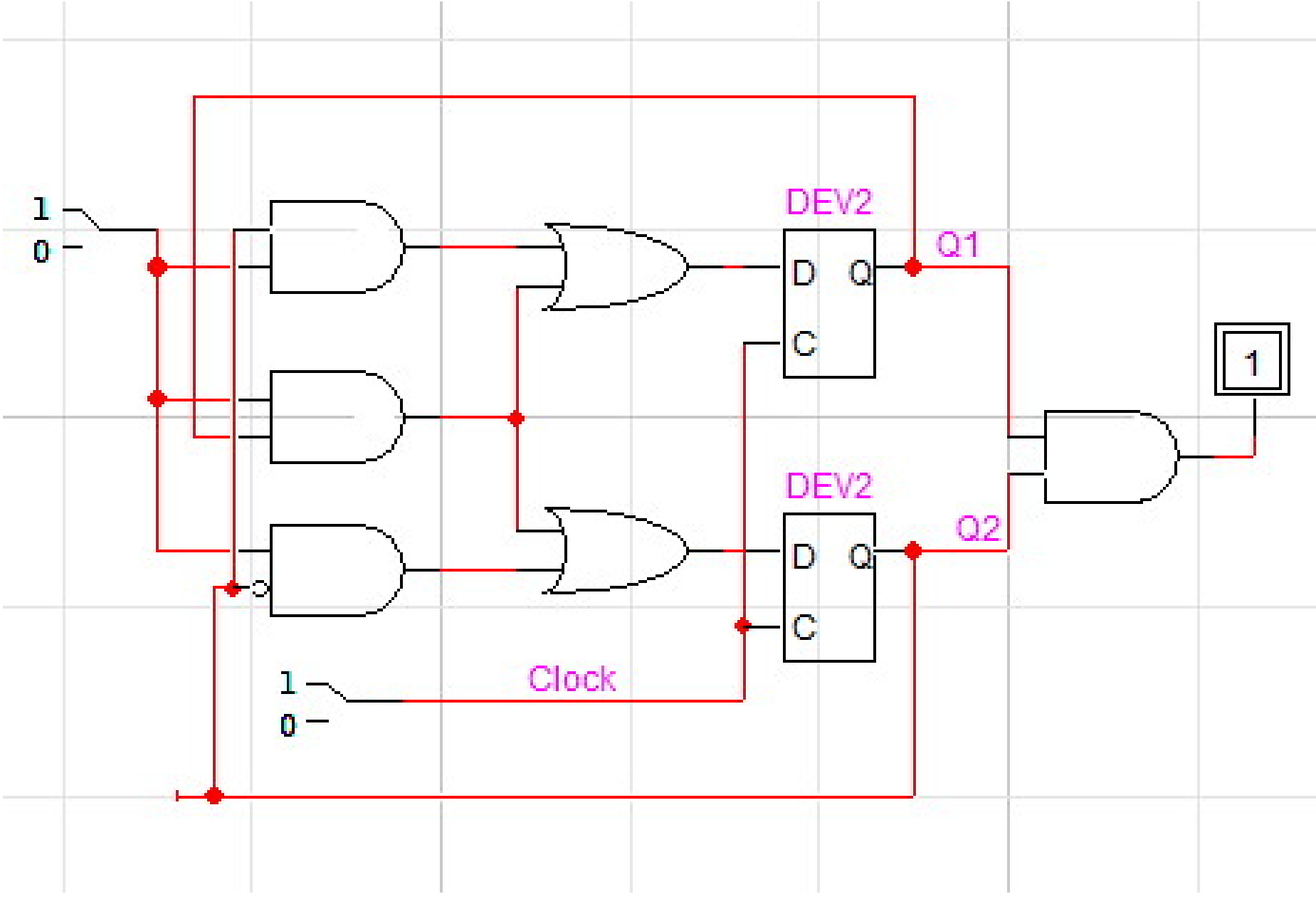
Output equation

The output depends **only** on the current state.



$$F = q_1 q_2$$

The circuit — with D-FFs



T Flip-Flop

Definition (T Flip-Flop)

The state is complemented if $T = 1$, it stays the same if $T = 0$.

T Flip Flop truth table

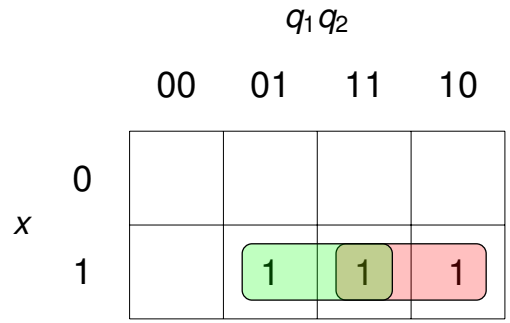
T	Q_{n+1}
0	Q_n
1	$\overline{Q_n}$

Problem

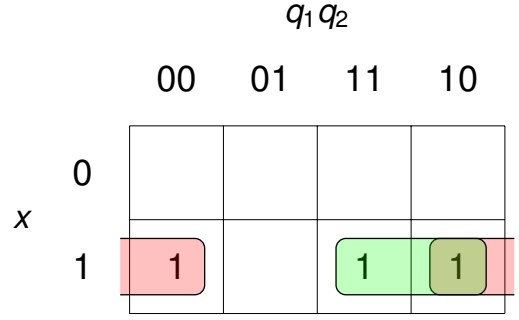
Draw the Karnaugh maps for T-FF.

T Flip-Flop

D-FF

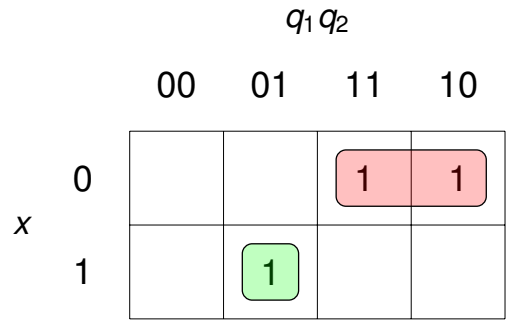


$$q_1^* = xq_1 + xq_2$$

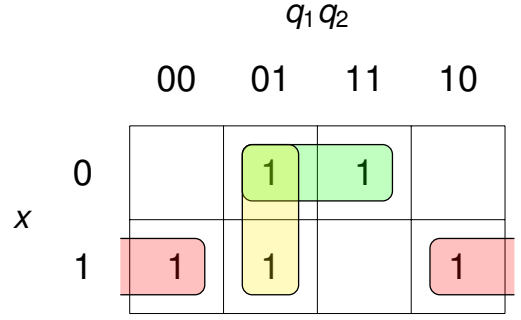


$$q_2^* = xq_1 + x\overline{q_2}$$

T-FF



$$q_1^* = \overline{x}q_1 + x\overline{q_1}q_2$$



$$q_2^* = \overline{x}q_2 + \overline{x_1}x_2 + x\overline{q_2}$$

K-map Transformation Rules: from D to T

Given a K-map for the next state variable x for a D-FF, do the following:

1. for all map entries where $x = 0$, transfer the values to the K map for the T-FF
2. for all map entries where $x = 1$, transfer the **complemented** values to the K map for the T-FF

For example, in the previous slide the first two columns for q_1^* (where $q_1 = 0$) are the same, and the last two are complemented.

JK-FF Behavioural Table

J	K	q	q^*
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

JK-FF Behavioural Table

J	K	q	q^*
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

J	K	q^*
0	0	q
0	1	0
1	0	1
1	1	$\overline{q}$

Example

Problem

Design a Moore Machine that will output a 1 iff they have been 2 ones followed by a zero and a one.

1. draw the state diagram
2. write the next state table (include output)
3. find a state assignment
4. state table to Karnaugh maps (depends on FFs used)
5. find the equations
6. draw the circuit

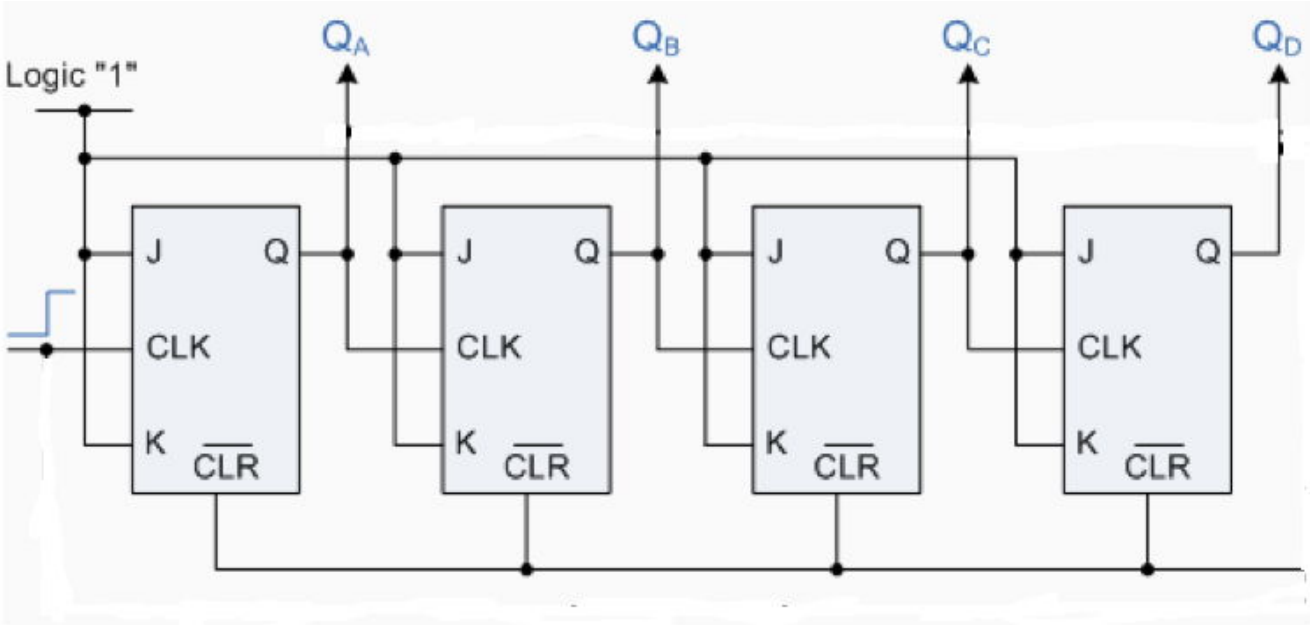
Design of an Synchronous Counter

Problem

Design a 4-bit counter (follow standard procedures)

1. use D-FF
2. use T-FF
3. use JK-FF
4. compare the designs
5. can you generalize?

Design of an Asynchronous Counter



NOTE: The FFs are negative edge sensitive.

Problem

Modify the counter to count $0, 1, \ldots, 8, 9, 0, 1, \ldots$

References

- https://bob.cs.sonoma.edu/IntroCompOrg-RPi/sec-seqdes.html
- https://www.allaboutelectronics.org/jk-flip-flop-explained-race-around-condition-in-jk-flip-flop-jk-flip-flop-truth-table-excitation-table-and-timing-diagram/