Sequential Circuits

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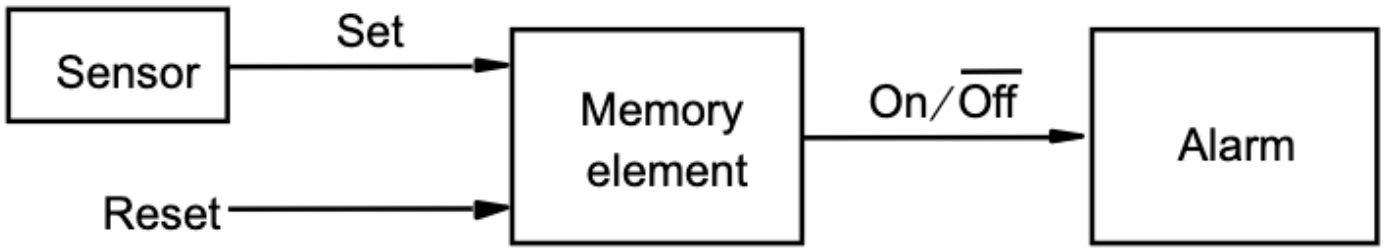
Sequential Circuits

The current output of a sequential circuit depends on the current input and the current state of that circuit

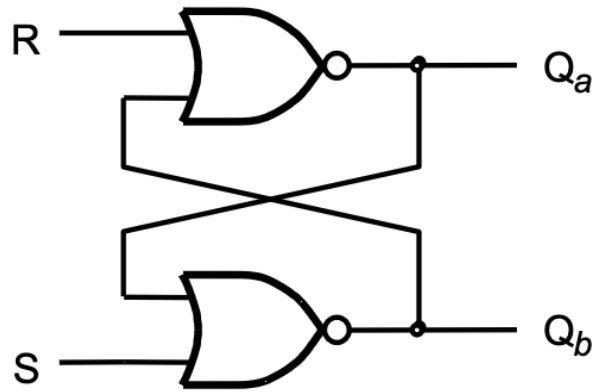
The circuit contains storage elements

It is basically a combinational circuit with a memory component



Flip-Flops

- A form of sequential circuit
- Characteristics of flip-flops:
  - It is a bistable device, exists in two states
  - Has two outputs, that are complements of each other
  - Constructed with NAND or NOR gates



(a) Circuit

S	R	Q_a	Q_b	
0	0	0/1	1/0	(no change)
0	1	0	1	
1	0	1	0	
1	1	0	0	

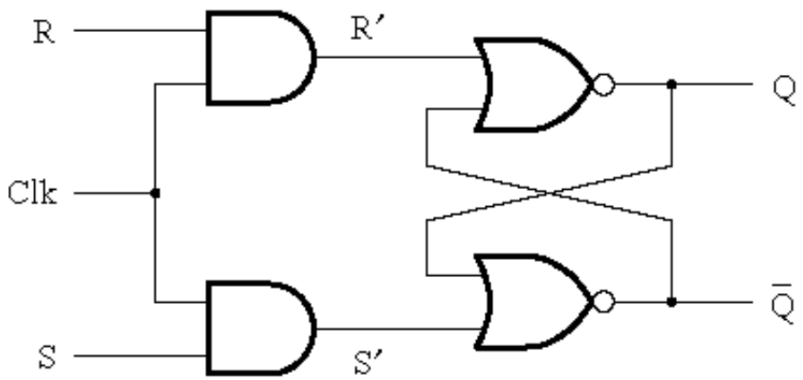
(b) Truth table

SR Latch

R	S	Q_{n+1}	$\overline{Q}_{n+1}$	
0	0	Q_n	$\overline{Q}_n$	previous state
0	1	1	0	set Q to 1
1	0	0	1	reset Q to 0
1	1	0	0	forbidden

Clocked SR flip-flop

- In the basic SR latch, the state changes only on input change
- For more control we need to add a clock to the latch to change state at particular times
- Problem with the SR latch: a spike in S or R will set/reset Q
- Solution: only allow S or R to change when the clock is low



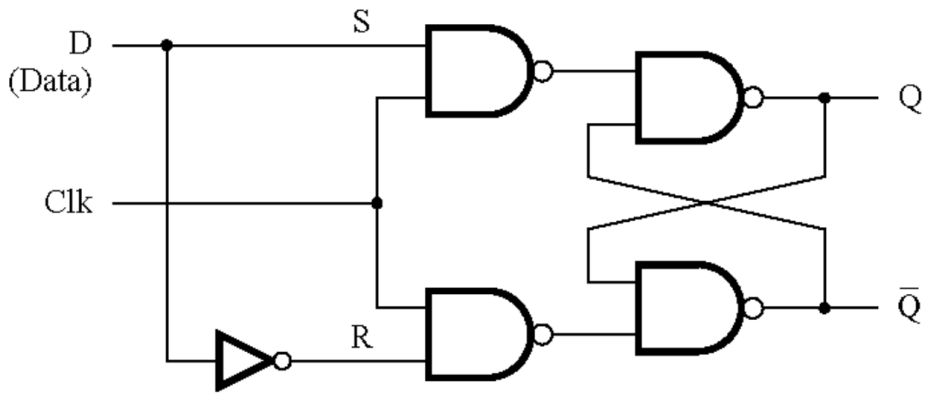
(a) Circuit

Clk	S	R	Q(t + 1)
0	x	x	Q(t) (no change)
1	0	0	Q(t) (no change)
1	0	1	0
1	1	0	1
1	1	1	x

(b) Characteristic table

Gated D latch

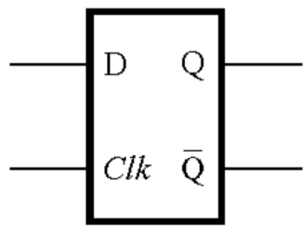
- The condition R = 1, S = 1 must be avoided (allow one input)
- Has one input instead of two
- Capture the data when the clock is high
- As long as the E is high the output changes according to the input



(a) Circuit

Clk	D	Q(t + 1)
0	x	Q(t)
1	0	0
1	1	1

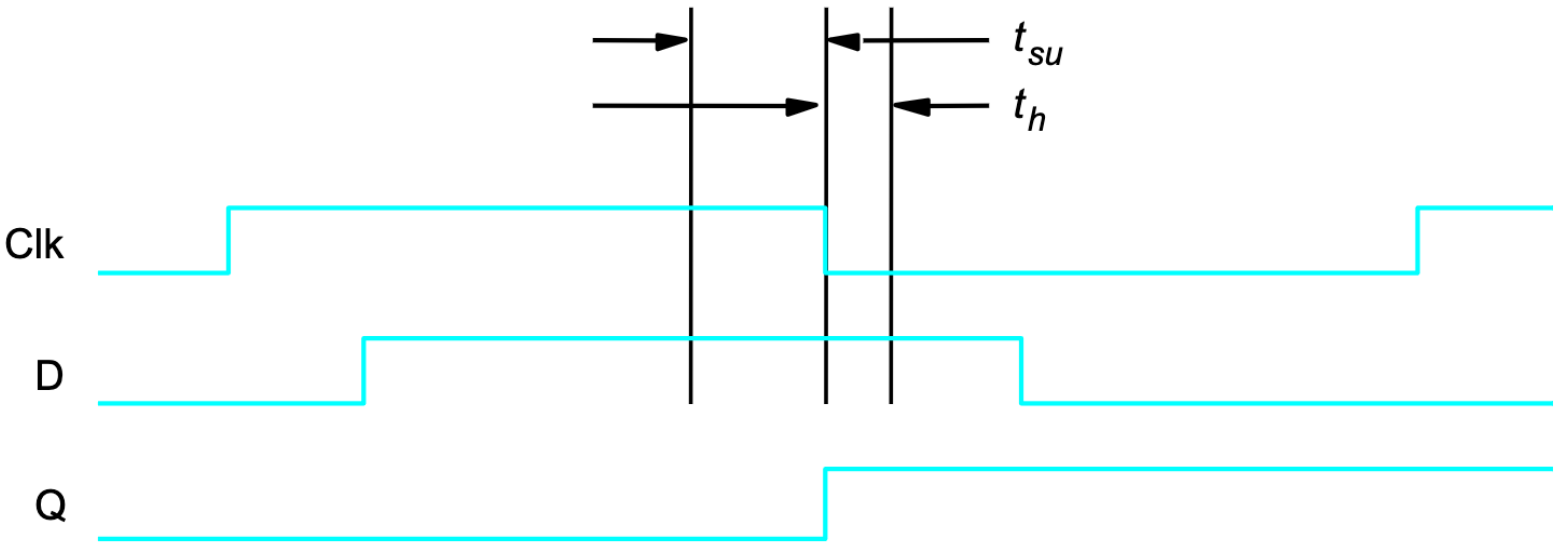
(b) Characteristic table



(c) Graphical symbol

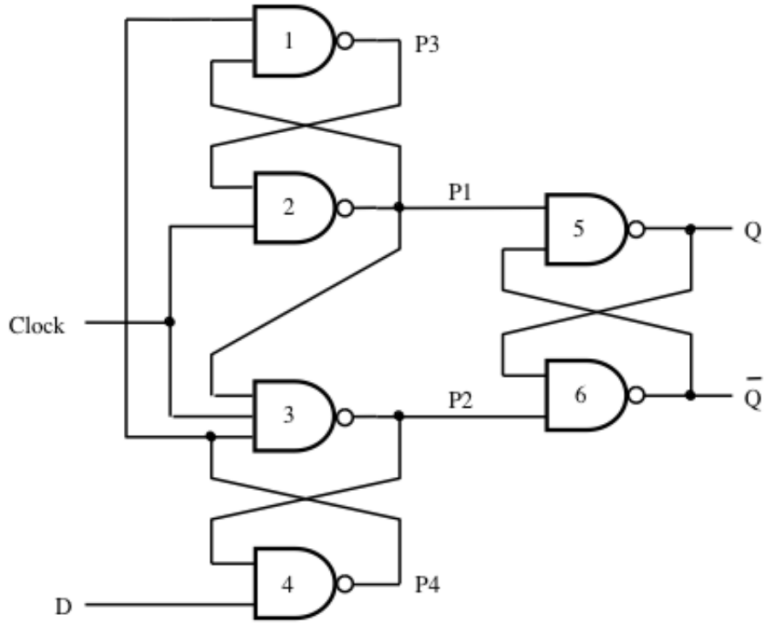
Edge Triggering

- Design storage elements where the output changes only when the clock changes
- These circuits are called edge triggered
- Propagation delay for a D latch:
  - Stores the value of D input at the time clock goes from 1 to 0
  - Operates properly if input is stable (not changing) at the time clk goes from 1 to 0

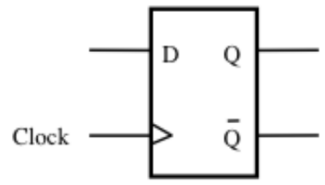


Positive-edge-triggered D flip-flop

- The output should only change once during a clock cycle
- Change on the edge of a cycle
- This can be accomplished as follows (master-slave)
- Master, changes its state when clk=1
- Slave, changes its state when clk=0



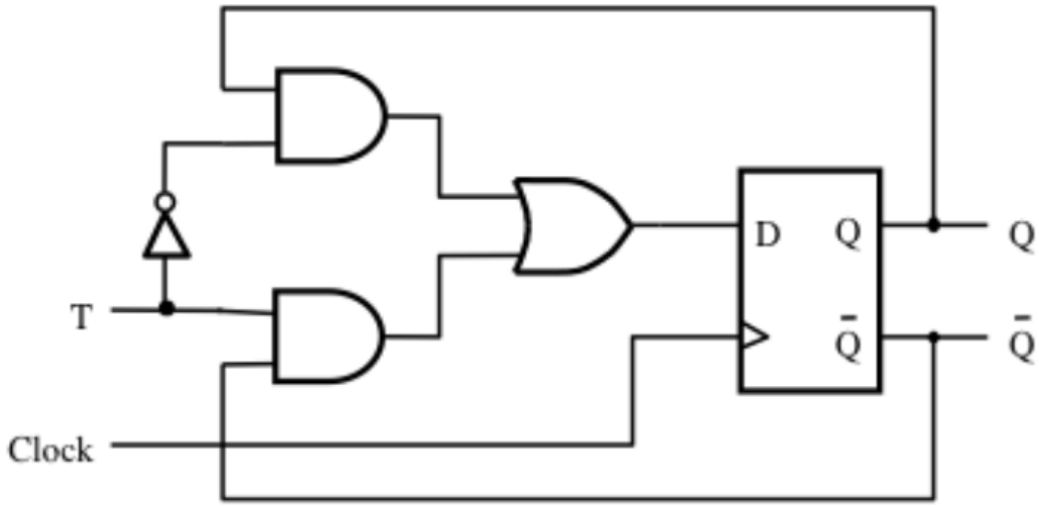
(a) Circuit



(b) Graphical symbol

Positive-edge-triggered T flip-flop

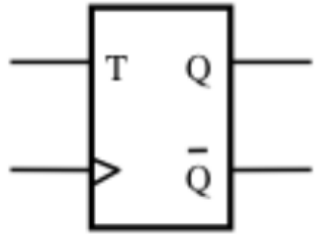
- The output "flips" if $T = 1$; no change if $T = 0$



(a) Circuit

T	Q(t + 1)
0	Q(t)
1	$\overline{Q}(t)$

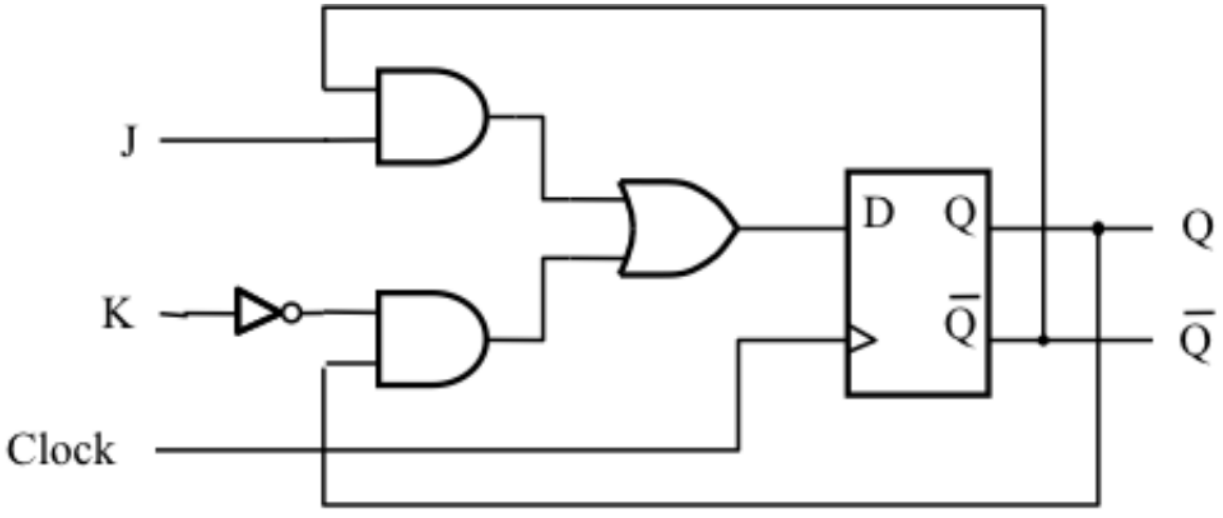
(b) Truth table



(c) Graphical symbol

Positive-edge-triggered JK flip-flop

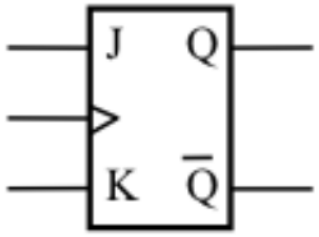
- J=S and K=R and behaves like a SR flip-flop
- Except all states are valid
- This is achieved by toggling the output



(a) Circuit

J	K	Q (t+1)
0	0	Q (t)
0	1	0
1	0	1
1	1	$\overline{Q}$ (t)

(b) Truth table

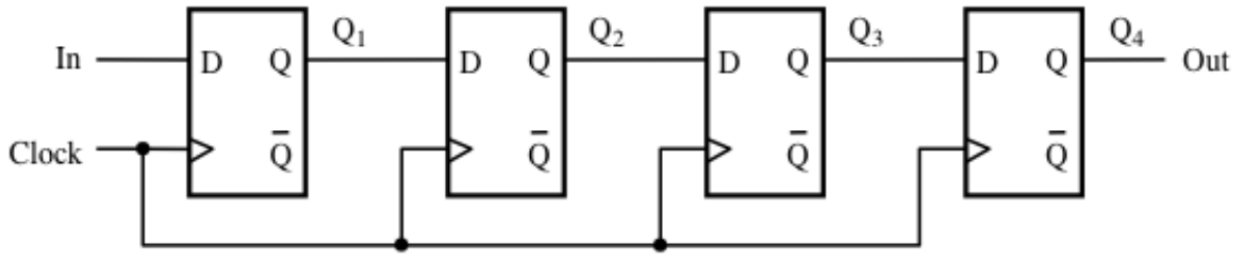


(c) Graphical symbol

Registers

- A number of flip-flops used to store bits of data i.e, n flip-flops store n bits information
- Two kinds of registers:
  - **Shift Registers:** accept and/or transfers data serially
  - **Parallel Registers:** has a set of 1-bit memories that can be read or written simultaneously

Shift Register

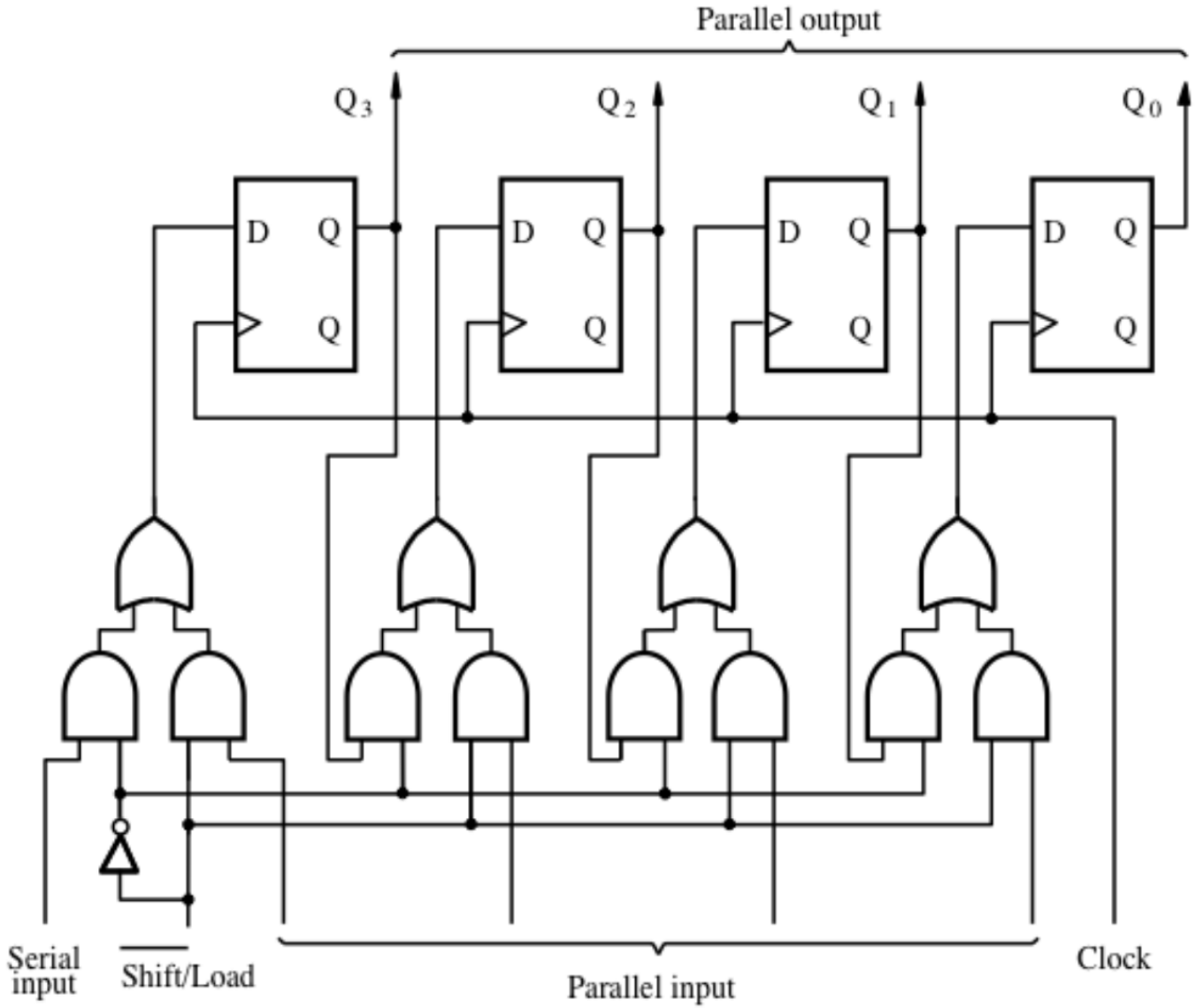


(a) Circuit

	In	Q_1	Q_2	Q_3	Q_4 = Out
t_0	1	0	0	0	0
t_1	0	1	0	0	0
t_2	1	0	1	0	0
t_3	1	1	0	1	0
t_4	1	1	1	0	1
t_5	0	1	1	1	0
t_6	0	0	1	1	1
t_7	0	0	0	1	1

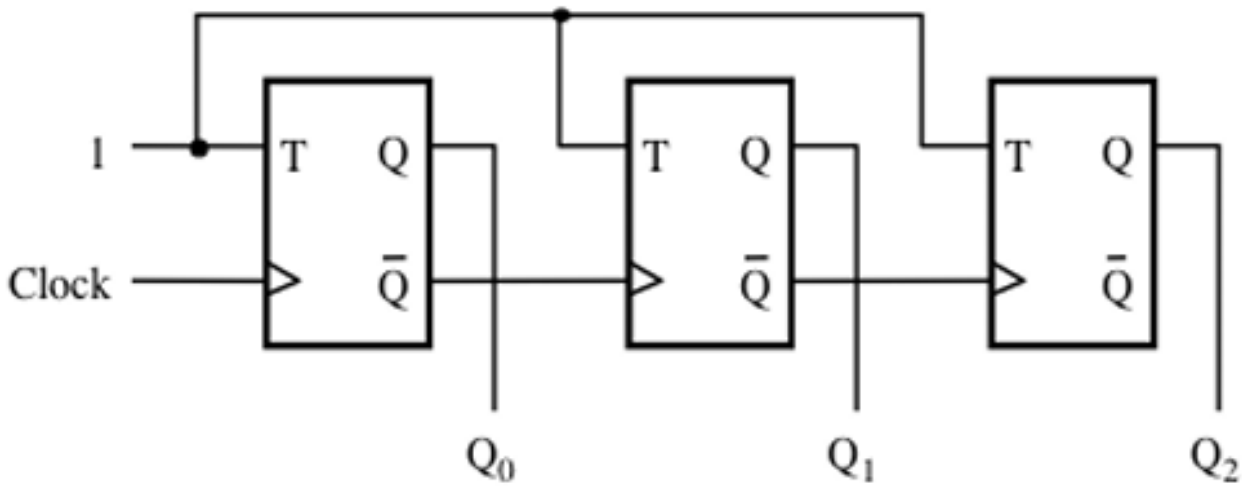
(b) A sample sequence

Parallel Register



Counters

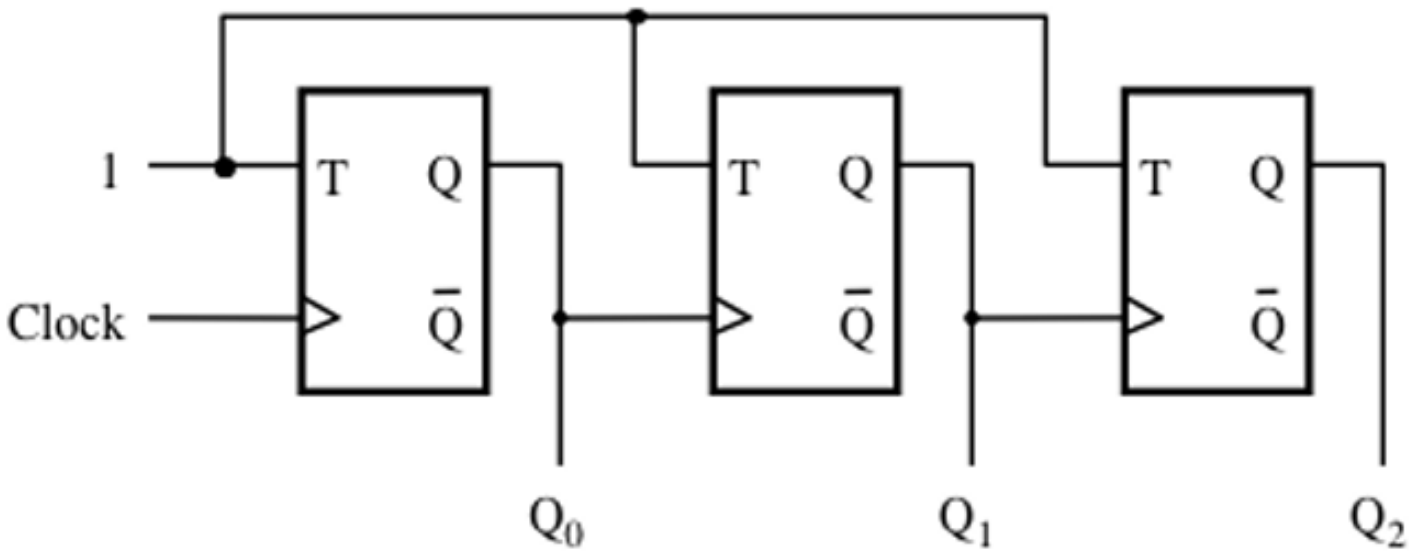
- Circuits that can increment or decrement a count by 1
- Can be built with T and D flip-flops
- Counters can be:
  - asynchronous
  - synchronous



(a) Circuit

Asynchronous Counters

- In our example a counter has three flip-flops but can have more latches
- The first flip-flop is the only one that is clocked (attached to the clock)
- The other flip-flops experience a propagation delay that affects their response

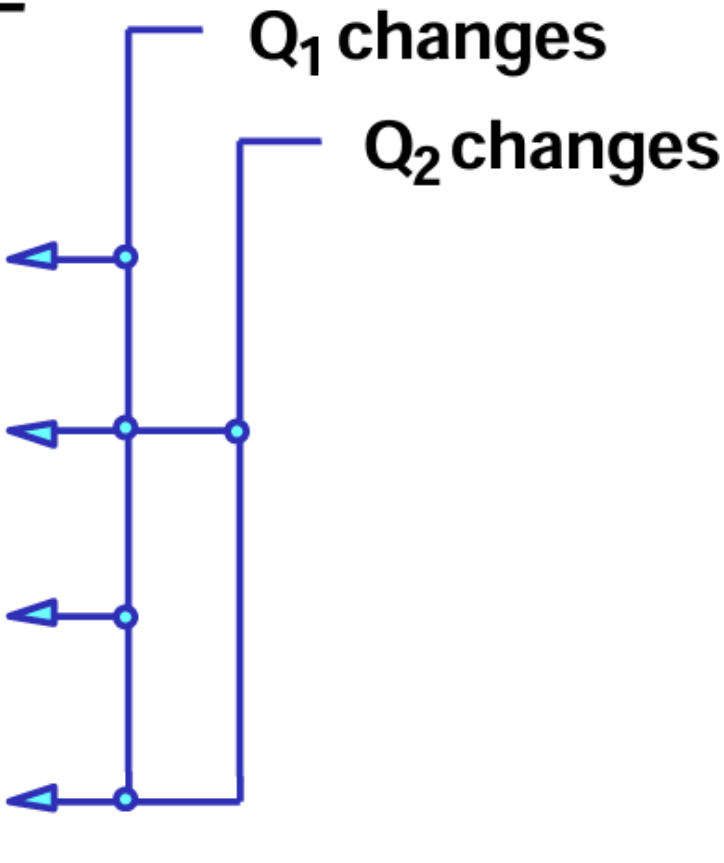


(a) Circuit

Synchronous Counters

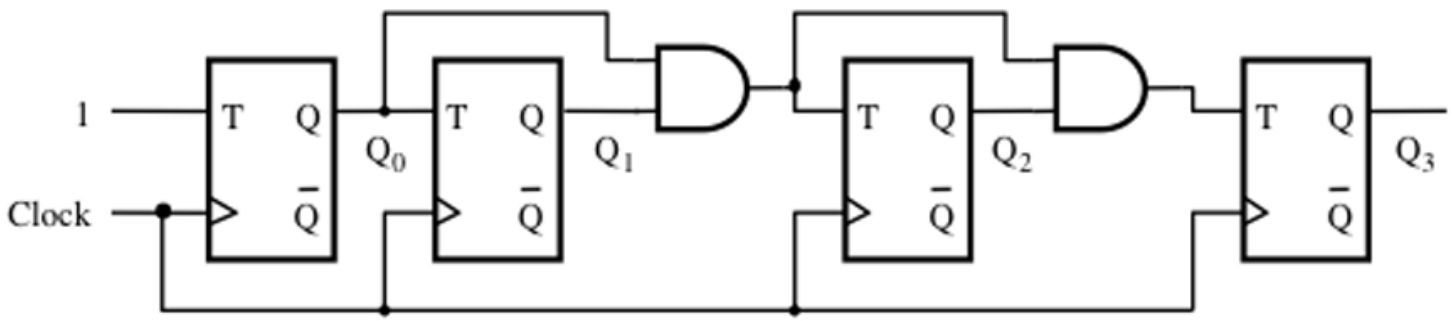
- Solves the challenges for asynchronous counters
- By clocking all the flip-flops at once

Clock cycle	Q_2	Q_1	Q_0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8	0	0	0



Synchronous Counters

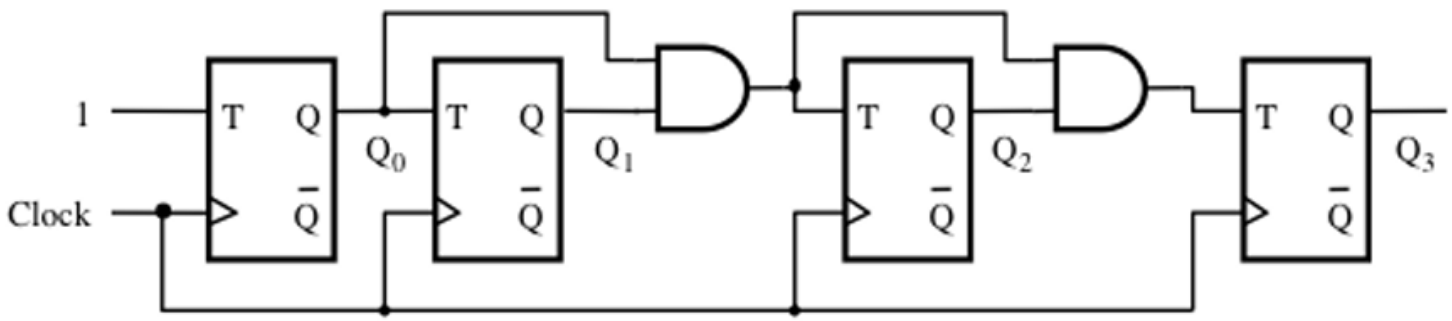
- Q0 is triggered on each clock cycle
- Q1 is triggered when Q0=1
- Q2 is triggered when Q1=1 and Q0=1



(a) Circuit

Synchronous Counters

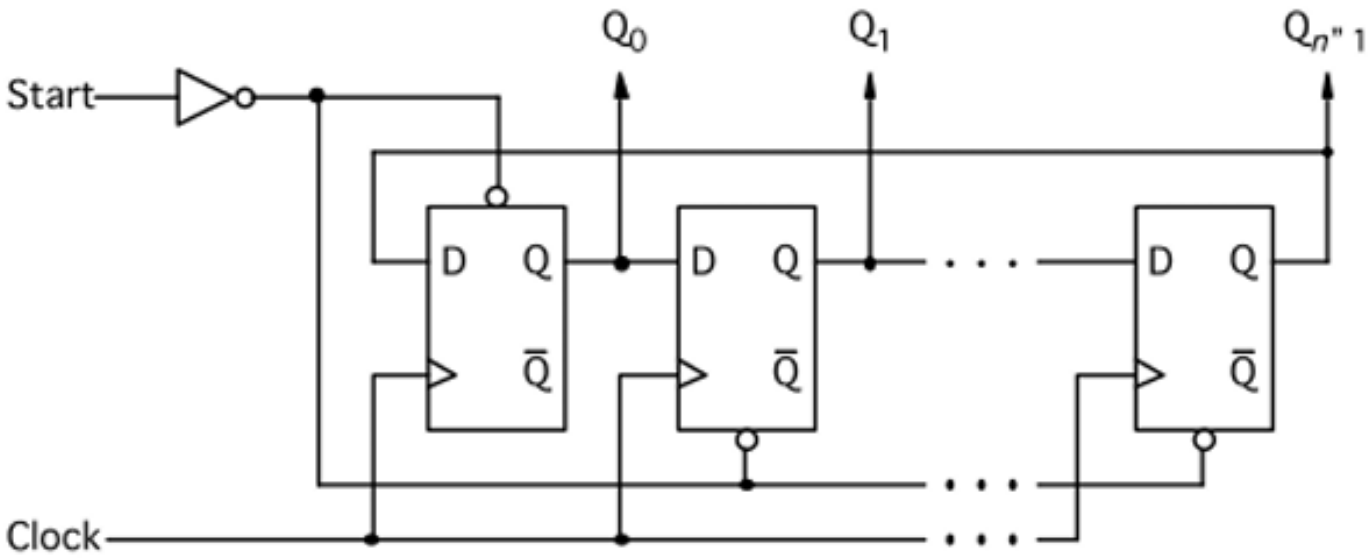
- $T_0 = 1$
- $T_1 = Q_0$
- $T_2 = Q_0 Q_1$
- $T_3 = Q_0 Q_1 Q_2$



(a) Circuit

Ring Counter

- Counters usually have state in flip-flops
- For ring counters, the output of the last flip-flop is connected as an input to the first flip-flop
- The non-complemented output is the one that is connected back to the input



(a) An *n*-bit ring counter

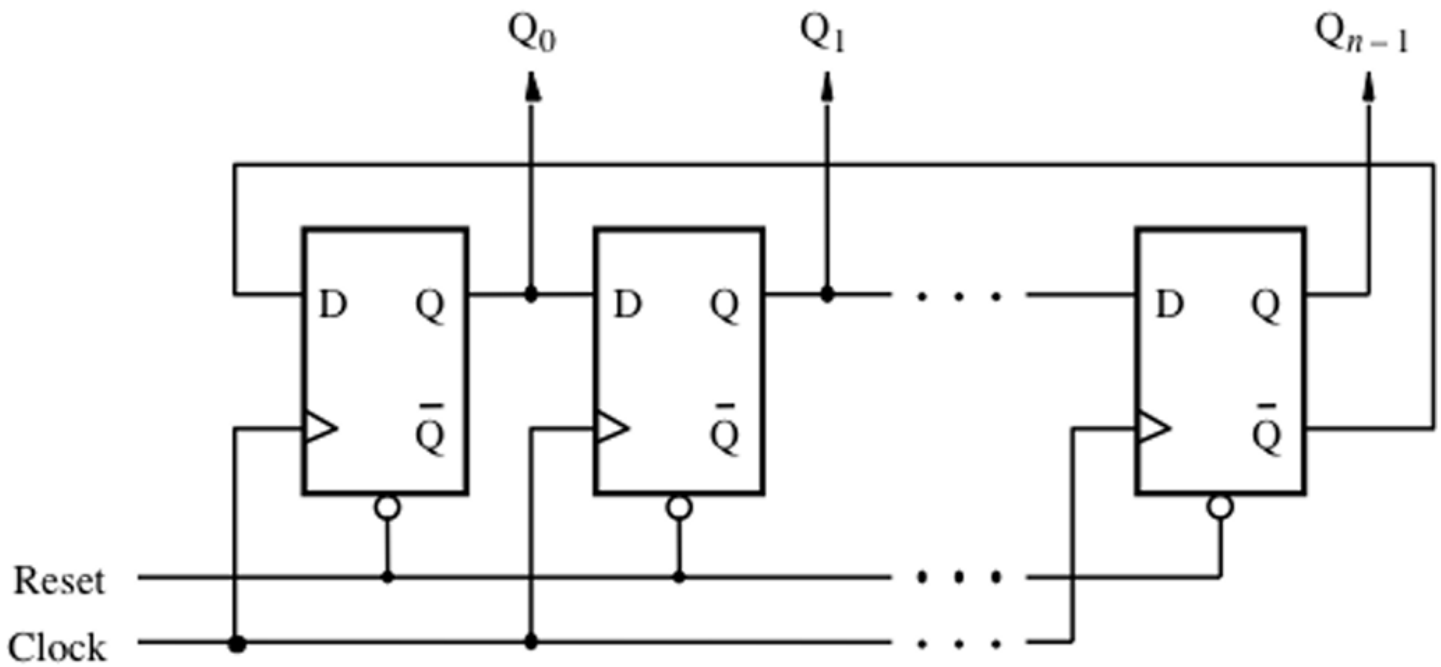
Ring Counter

- Can be made of D-flip flops or JK-flip flop
- Has Mod = n, *n* is the number of bits
- That is 4-bit ring counter has 4 states
- Only 4 of the 15 states are utilized

States	Q_A	Q_B	Q_C	Q_D
1	1	0	0	0
2	0	1	0	0
3	0	0	1	0
4	0	0	0	1

Johnson Counter

- Twisted Ring counter
- Complemented output of the flip-flop is connected with the input of the first flip-flop
- Can also be built with D-flip flops or JK-flip flops



Johnson Counter

- Has Mod = 2n, n is the bit size of the counter
- It therefore counts to a sequence of length 2n
- Utilizes the maximum number of states

States	Q_A	Q_B	Q_C	Q_D
1	0	0	0	0
2	1	0	0	0
3	1	1	0	0
4	1	1	1	0
5	1	1	1	1
6	0	1	1	1
7	0	0	1	1
8	0	0	0	1

References

- https://www.ece.mcmaster.ca/ xwu/2di4/chapter7.pdf