

University of New Brunswick
Computer Science
Computer Architecture and Organization
Instructor: Joanna Nanjekye, jnanjeky@unb.ca
Due Date: August 9, 2024 – 11:59 PM

LAB 4 – OPTIONAL LAB

Pre-lab instructions:

- Complete and test the setup required for the remote access to the FCS labs: <https://www.cs.unb.ca/help/>
 - Set up UNB VPN: <https://unbcloud.sharepoint.com/sites/ITServices/SitePages/VPN.aspx>
 - Set up SSH for the command line mode access: <https://www.cs.unb.ca/help/ssh-help.shtml>
 - Set up VNC for the remote desktop access: <https://www.cs.unb.ca/help/remote-lab-gui-access.shtml>
- Start a VNC session before the lab session.

Reference materials

- LogicWorks 5, by Capilano Computing Systems, Benjamin-Cummings. Chapter 4, pages 21 to 33, provides a tutorial with advanced features.
- Sample LogicWorks tutorial online: <https://www.cs.uregina.ca/Links/class-info/201/LW5/lecture.htm>

General instructions:

- Log in to Windows in the FCS lab.
- Using remote access to the FCS labs is recommended.
- Complete lab exercises and prepare a lab report.
- Group work is allowed, however, individual D2L submissions are required from each student.
- You may finish the lab on your own time.

Submission instructions:

- Submit the pdf files to the Desire2Learn dropbox

Task 1. Design a 3-bit up/down counter. If the input $up = 1$ the counter will count up, otherwise it will count down. Use T-FF. Show how this can be expanded to a 4-bit counter.

- Simulate the circuit using LogicWorks and create a pdf file of the circuit

Task 2. Design a circuit that recognizes an input sequence that has at least two consecutive 1's or two consecutive 0's. The recognizer has a single output Y. There also should be asynchronous reset. For example:

input: 001111101010011000011101
Y: 001011110000010101110110

- Simulate the circuit using LogicWorks and create a pdf file of the circuit