

University of New Brunswick
Computer Science
Computer Architecture and Organization
Instructor: Joannah Nanjekye, jnanjeky@unb.ca
Due Date: August 2, 2024 – 11:59 PM

LAB 2 EXTENDED

Pre-lab instructions:

- Complete and test the setup required for the remote access to the FCS labs: <https://www.cs.unb.ca/help/>
 - Set up UNB VPN: <https://unbcloud.sharepoint.com/sites/ITServices/SitePages/VPN.aspx>
 - Set up SSH for the command line mode access: <https://www.cs.unb.ca/help/ssh-help.shtml>
 - Set up VNC for the remote desktop access: <https://www.cs.unb.ca/help/remote-lab-gui-access.shtml>
- Start a VNC session before the lab session.

Reference materials

- LogicWorks 5, by Capilano Computing Systems, Benjamin-Cummings. Chapter 4, pages 21 to 33, provides a tutorial with advanced features.
- Sample LogicWorks tutorial online: <https://www.cs.uregina.ca/Links/class-info/201/LW5/lecture.htm>

General instructions:

- Log in to Windows in the FCS lab.
- Using remote access to the FCS labs is recommended.
- Complete lab exercises and prepare a lab report.
- Group work is allowed, however, individual D2L submissions are required from each student.
- You may finish the lab on your own time.

Submission instructions:

- Submit the pdf files to the Desire2Learn dropbox

Task 1. Design a sequential circuit with 2 JK flip-flops A and B and two inputs E and x. If $E = 0$, the circuit remains in the same state regardless of the value of x. When $E = 1$ and $x = 1$, the circuit goes through the state transitions from 00 to 01 to 10 to 11 back to 00 and repeat. When $E = 1$ and $x = 0$, the circuit goes through the state transitions from 00 to 11 to 10 to 01 back to 00 and repeat.

- Submit a circuit diagram for this problem

- Provide a truth table for positive-edge triggered J K flip flop
- Provide a truth table for negative-edge triggered J K flip flop

Task 2. Modify the schematic of the master/slave flip-flop to include an ability to asynchronously preset (force Q to one) or preclear (force Q to zero) the outputs. By asynchronous, we mean that the function takes place independently of the clock signal.

- Draw the schematic
- Verify its proper operation through simulation.