University of New Brunswick

Computer Science

CS3853: Computer Architecture and Organization

Instructor: Joannah Nanjekye, jnanjeky@unb.ca

Due Date: July 26, 2024 —- 11:59 PM

ASSIGNMENT 2

Submission instructions:

- Submit a pdf file to the Desire2Learn dropbox

Problem 1. Find the respective expressions for following Boolean functions using Karnaugh maps:

- F(A,B,C) = $\sum$m(0, 1, 2, 3, 4, 6)
- F(A,B,C) = $\sum$m(0, 4, 6, 7)
- F(A, B, C, D) = $\sum$m(0, 1, 2, 5, 6, 7, 8, 10, 13, 15)
- F($w_1, w_2, w3, w_4$) = $\prod$m(0, 2, 3, 8, 9, 11, 15) + $\sum$ d(4,5,6)
- F($w_1, w_2, w3, w_4$)= $\sum$m(4,6,8,10,11,12,15) + D(3,5,7,9)
- F(A,B,C,D,E) = $\sum$m(0,1,2, 3, 4, 6,12,14,15,16,17,18,20,24,28,30,31)

Problem 2. Find the respective expressions for following Boolean functions using the Quine-McCluskey tabular algorithm:

- F(A, B, C) = $\sum$m(0, 1, 2, 3, 4, 6)
- F($w_1, w_2, w3, w_4$)= $\sum$m(4,6,8,10,11,12,15) + D(3,5,7,9)
- F(A,B,C,D,E)= $\sum$m(0,1,2, 3, 4, 6,12,14,15,16,17,18,20,24,28,30,31)
- F(A,B,C,D,E) = $\sum$m(3,5,6,9,10,11,13,19,21,22,23,25,26,27,29)

Problem 3. Consult the class notes (slides) and discussion on flip-flops to implement the following. In each case use any additional logic gates that are required.

- A T-FF using a D-FF
- A JK-FF using a T-FF
- A D-FF from a JK-FF
- A JK-FF using a D-FF

Problem 4. Design an FSM that recognizes 10111 or 10101.

- Draw state transition diagram (use as few states as possible).
- Choose state encodings.
- Write state transition and output table using the encodings.
- Write next state equations and output equations.

Problem 5. Design a 3-bit up/down counter. If the input $up = 1$ the counter will count up, otherwise it will count down. Use T-FF. Show how this can be expanded to a 4-bit counter. No formal methods are needed for this problem.

Problem 6. Design a circuit that recognizes an input sequence that has at least two consecutive 1's or two consecutive 0's. The recognizer has a single output Y. There also should be asynchronous reset. For example:

```
input:  001111101010011000011101
Y:      001011110000010101110110
```

- Devise the state diagram
- Encode the states
- Obtain the equations for D flip-flops
- Simulate the circuit using LogicWorks (this is done in Lab 2—nothing needs to be handed in here.)

Problem 7. Design an asynchronous counter using a D-FF and one input x. If x = 0 it counts 1,2,3, 0, 1,2 . . .; if x = 1 it counts 1, 3, 0, 1, 3, ... Assume that x only changes in 1 or 3 (in which case there are two combinations that will never occur – state 2 and x = 0 and state 0 and x = 1).

Problem 8. Design a sequential circuit that simulates the operation of a traffic light system. Use a JK-FF and and any others logic gates required. The state machine for this has 8 states. The initial state has to be red state. It should stay in that state for at least 4 clock cycles. Then it goes to the green state for at least 3 clock cycles. Finally it goes to yellow state for one clock xylem before going back to red state. To ensure the state machine starts in red state, it will need to have a single "reset" input that will set all of the d flip flop to the correct value. Additionally, it should have an input, which when asserted will allow the state machine to cycle to the red state but then stay there until input is de-asserted.