Investigating FPGA Architectures for System-on-Chip

Jingjing Li / Kenneth B. Kent
University of New Brunswick
Faculty of Computer Science
d5k48@unb.ca ken@unb.ca

Outline

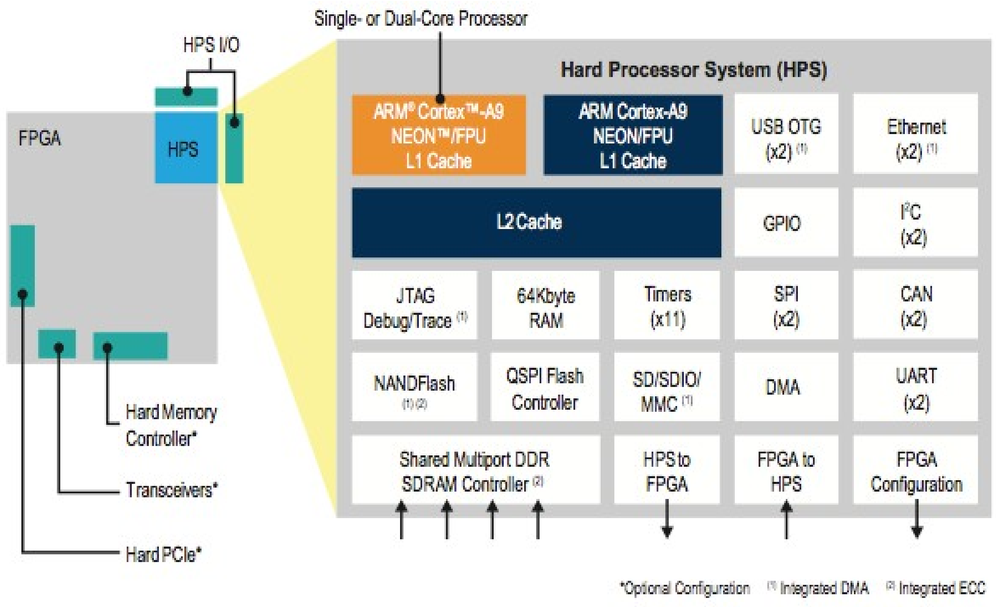
- **Adapting an Arm processor to work in the VTR project.**
- **Verifying the correctness of the processor through simulation.**
- **Measuring the suitability of various FPGA architectures for System-on-Chip designs.**

Motivation

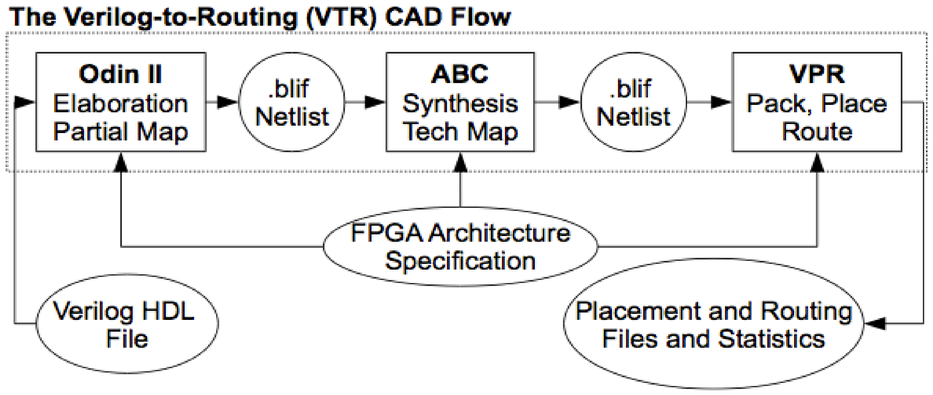
Field Programmable Gate Arrays (FPGA) are an integrated circuit which can be programmable. System-on-Chip puts all main components of a computer into a single chip. The goal of this project is to explore FPGA architectures and support System-on-Chip processor research in VTR. The proposed FPGA architectures will have a new feature to extend the applications. Not only the production cost and system power will be reduced, but also the FPGA space utilization will be increased.

Background

A basic design of an FPGA consists of I/O blocks and logic blocks surrounded by programmable routing. It can be programmable and tested immediately. For the logic blocks, there are two types: soft logic blocks and hard logic blocks. Soft logic blocks can be re-programmable and used for other functional circuits. Hard logic blocks can not be re-programmable, but the speed is faster and power is much lower.



The Verilog-to-Routing (VTR) Computer Aided Design (CAD) workflow is an available FPGA CAD flow. This CAD flow includes ODIN II which performs front-end synthesis, ABC which performs logic and physical synthesis, and VPR which performs packing, placement and routing to the target FPGA architecture.



Methodology

In this project, we are using the Arm core processor amber25 as the implementation case.

- **Arm core processor is a large verilog circuit design. The processor can be divided into several components. Each components of the verilog design needs to be examined by itself. ODIN II can debug the verilog design, do some pre-processor to support verilog language and produce the output correctly.**
- **To verify the correctness of the processor, programs should be run on the Arm core processor. We also need to write programs to load application into memory for memory initialization. According to the simulation, we can verify the results.**
- **To determine suitable FPGA architecture, we can experiment with Arm core processor circuits on the FPGA successfully and obtain measurements of designs for different architectures.**

Result

- **Through VTR workflow, we can obtain measurements from the input Arm core verilog design based on the performance of FPGA architectures. But we are not sure if the result is correct. By using a simulator of the System-on-Chip, we can verify the correctness of the results. Odin II provides a simulator that will have to be extended to support SoC simulation.**