Improving Memory and Validation Support in FPGA Architecture Exploration

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Introduction

Field-programmable gate array (FPGA) researchers require support for Verilog hardware description language (HDL) in order to support ongoing FPGA architecture exploration. ODIN II is a Verilog HDL compiler developed for this purpose.

To support research in this area, ODIN II must be demonstrated to be correct. It must also adequately support important FPGA constructs such as memories and multipliers.

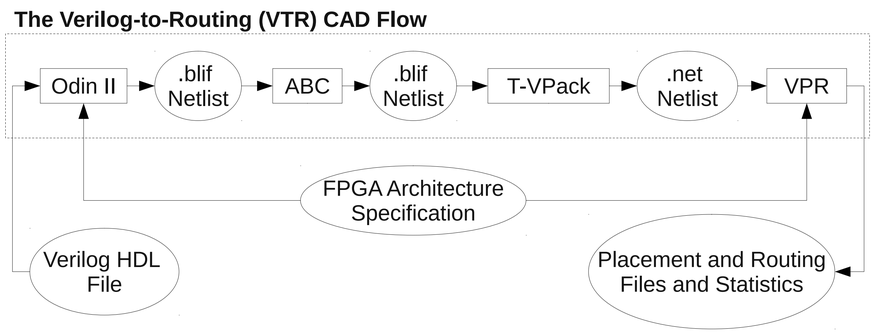
Current research involves:

- Fast parallel simulation in ODIN II
- Verification of ODIN II through simulation
- Support for architecture-aware memory splitting
- Soft logic memory support
- Implicit memory support
- Examining the benefits of soft vs. hard block memories for various circuits and architectures.
- Comparing placement and routing results using ODIN II's memory splitting vs. VTR's packing.

Background

An FPGA is a reconfigurable chip which is capable of behaving like an arbitrary digital circuit as described by its programming. FPGAs consist of lookup tables (LUTs) and an interconnection fabric consisting of wires and programmable switches.

FPGAs can also contain hard blocks, or regions of fixed-function logic which perform specific operations more efficiently. Examples of hard blocks are memories and multipliers.

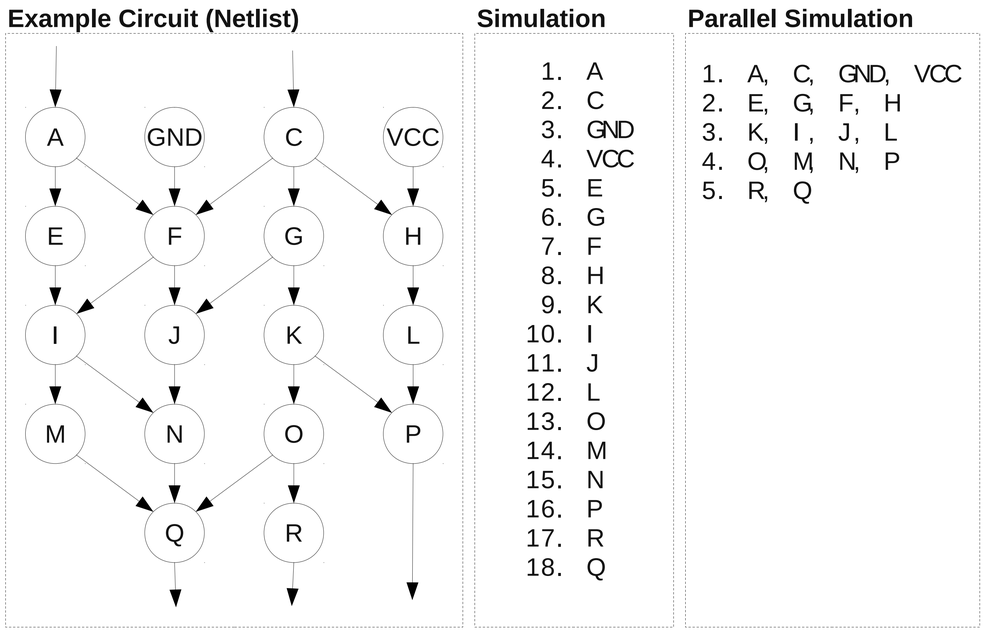


The Verilog-to-routing (VTR) computer aided design (CAD) flow gives researchers the ability to explore hypothetical FPGA designs. This CAD flow includes ODIN II which performs high level synthesis (Verilog compilation), ABC which performs reduction (synthesis), T-VPack which performs logic block clustering, and VPR which places and routes the circuit to the target FPGA.

Solution

Simulation was previously performed by repeated traversal of the netlist. However this technique is wasteful since the order never changes.

Parallel simulation can easily be accomplished by staging the ordered nodes according to their dependencies. Each stage may be then be computed in parallel.



Verification of ODIN II and the simulator may be accomplished by comparing the simulation results from ODIN II with the results from a commercial simulation tool such as ModelSim.

With reliable and fast verification in place, supporting new features becomes easier. Architecture-aware memory splitting requires taking the memory width and depths from the architecture specification data structures within ODIN II and splitting or padding the memories to these specifications.

Soft logic memory support requires a modification of the partial map to the target device to allow memory blocks to be expanded into soft logic.

Implicit memory support requires that the semantic analysis stage of ODIN II's compiler be modified to support the building of a memory block under certain conditions. Initially this will be done whenever a 2D register is encountered.

Results

The improved sequential simulation algorithm provides us with a substantial (>2x) performance improvement over repeated traversal as the number of cycles simulated increases. Parallel simulation gives us a speedup of over 2.2 with four processors when compared with the improved sequential algorithm.

Development of improved memory support is complete. Further experiments will be conducted to determine cut off points for soft logic vs. hard block memory on various architectures, and to compare ODIN II's splitting with VTR's when packing logical memories into physical blocks.