Acceleration of Blob Detection within Images in Hardware

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Outline

 Implementation and evaluation of image processing algorithms on FPGA architecture

Parallelization of image processing algorithms

Problem

Computer Vision tasks are required in many applications. We need to find a balance between high image resolution and fast processing speed. Most of the time either one of those needs to be shortened to fulfill the desired criteria.

The problem addressed in this project is the detection of binary large objects (blobs) in a continuous video stream and compute their center point. It is related to a project at the Bonn-Rhein-Sieg University of Applied Sciences in Germany where the invention of a multi user interaction device for 3D projection environments is ongoing.

- Experimental implementation of blob detection methods for evaluation purposes
- Computation of blob center point by bounding box and center of mass
- Comparison of performance and precision with similar solutions on General Purpose Processor architectures

Motivation

Invention of a passive tracking system for estimation of position and orientation of the user in virtual environments



By employing standard image processing algorithms on FPGA architectures we are working to achieve a performance gain for real-time interaction.

Solution

to greyscale The system performs a transformation from Pixel Analog color to greyscale. detection Video-In All pixels are processed Adjacency sequentially and proof tracked as part of a blob Merging of if their brightness is blobs VGA-Out above a defined thres-Computation of hold value. Selected pixels are checked for adjacency Output on to already detected blob 7-seg. display pixels in the current frame. Adjacent blobs are merged and their center point is computed by the bounding box method which is displayed on the seven-segment-display of the DE2 board.



Representation of the user by laser emitting device, projecting a unique pattern to allow 6 degrees of freedom

Material

Altera DE2 board with Cyclone II

Quartus II Web Edition (ver. 9.0)

- Implementation in SystemVerilog
- Simulation with Waveform files
- Compilation and programming



Results

For evaluating the performance the very same blob detection method has been implemented on a GPP architecture. It scanned the frame pixels sequentially and computed the blobs center points by bounding box measurement.

It could be shown that the FPGA approach can perform with at least 20 frames per second faster than the very same program logic on a GPP architecture. This also includes the additional video processing on the FPGA system to convert from analog to digital before performing the blob detection while the GPP system could directly grab whole frames from the digital video file.

The extension of the system by a center of mass based computation of the center point is going to be one of the next steps in the future.

Analog video input source providing simplified image material



The design of the immersion square requires the computation of three video streams in parallel, since all three sides of the cube need to be tracked. This and the parallelization aspect of the FPGA architecture for the processing of the single image frames have not been taken into account until now.

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